CLAIMS

What is claimed and desired to be secured by Letters Patent is:

1. A multi-port register file memory, the memory comprising:

at least one storage element;

at least one read port coupled to said storage element; and

a differential sensing device coupled to at least said read port and adapted to sense a predefined voltage swing.

2. The register file memory of claim 1, wherein the register file memory operates asynchronously.

3. The register file memory of claim 1, wherein the register file memory operates synchronously.

4. The register file memory of Claim 1, wherein said voltage swing is at least a portion of the total voltage supply.

5. The register file memory of Claim 4, where said voltage swing is about 100 millivolts typically.

6. The register file memory of Claim 1, wherein said voltage swing is defined relative to a top rail of a voltage supply.

7. The register file memory of Claim 1, wherein said differential sensing device is a two-stage analog-style sense amplifier.

8. The register file memory of Claim 7, wherein said two-stage analog-style sense amplifier includes at least one amplifier enhancing device.

9. The register file memory of Claim 7, wherein said two-stage analog-style sense amplifier includes at least one trip-level-shifted inverter device.

10. The register file memory of Claim 7, wherein said two-stage analog-style sense amplifier includes at least one power switch device adapted to turn off power to said two-stage analog-style sense amplifier.

11. The register file memory of Claim 7, wherein said two-stage analog-style sense amplifier includes a voltage reference device.

12. The register file memory of Claim 1, wherein said read port comprises a pair of transistors, wherein at least one transistor of said pair is larger with respect to another transistor of said pair.

13. A multi-port register file memory adapted to be used in applications where a power supply of less than about 1.08 volts occurs, the memory comprising:

at least one memory cell;

a differential sensing circuit adapted to sense a small voltage swing;

a voltage reference device coupled to said differential sensing circuit; and

a latched output coupled to differential sensing device.

14. The memory device of Claim 13, wherein said memory cell includes at least one storage element.

15. The memory device of Claim 13, wherein said memory cell further includes two read port pairs coupled to said storage element.

16. The memory device of Claim 15, wherein each of said read port pairs includes two transistors of different sizes.

17. The memory device of Claim 13, wherein said differential sensing circuit includes two amplifier enhancing devices.

18. The memory device of Claim 13 including more than one write port.

19. The memory device of Claim 13 including more than one read port.

20. A multi-port register file memory adapted to be used in applications where a power supply of less than about 1.08 volts occurs, the memory comprising:

a plurality of storage elements arranged in a plurality of rows and columns;

at least one read port and one write port coupled to each of said storage elements;

a differential sensing device adapted to sense a small voltage swing;

a voltage reference device coupled to said differential sensing device; and

a latched output circuit coupled to differential sensing device.

21. A multi-port register file memory, the memory comprising:

a plurality of storage elements arranged in rows and columns;

means for selecting one of said storage elements; and

means for differentially sensing a small bitline voltage swing.

22. A method for improving speed and increasing performance in a multi-port register file memory having a plurality of storage elements, the method comprising:

selecting at least one of the storage elements; and

differentially sensing a small voltage swing.

23. A method for reading data stored in a multi-port register file memory having a plurality of storage elements arranged in rows and columns, the method comprising:

selecting one of the storage elements;

flowing a current through at least one transistor of the memory cell in the selected storage element;

causing an output of a sense amplifier connected to at least one said selected memory cells to switch accessed data to full CMOS logic levels.